

USER'S GUIDE

QUADRASYNC

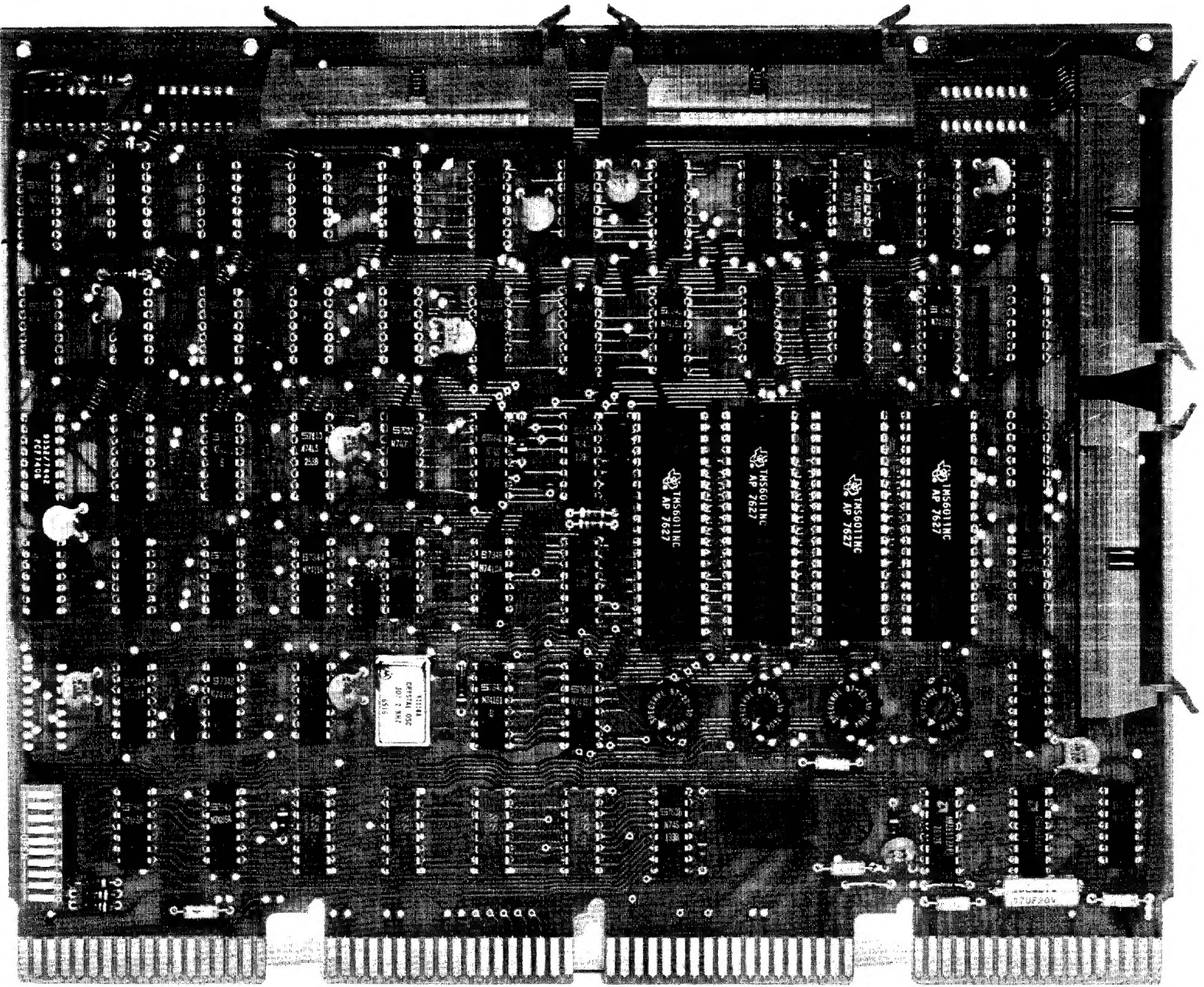
Model 10015

January 14, 1977

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By

ABLE COMPUTER TECHNOLOGY, Inc.



QUADRASYNC - Model 10015

QUADRASYNC SPECIFICATIONS

FUNCTION

Provides an interface between the PDP^{*}-11 Unibus^{*} and four asynchronous EIA Serial Communication Channels. Software compatible with the Digital Equipment Corporation DL-11B.

MECHANICAL

The QUADRASYNC^{**} consists of one quad module which can be installed in any Small Peripheral Controller (SPC) slot.

OPERATING MODE

Full duplex or half duplex communication capability the same as furnished with the DEC^{*} Model DL-11B.

DATA FORMAT

Asynchronous, EIA serial. One start bit, 8 data bits and one stop bit.
Low order bit first.

BUS LOADING

The QUADRASYNC presents one unit load to the Unibus.

ELECTRICAL INTERFACE

The QUADRASYNC provides a voltage level interface and on-board connectors whose signal levels conform to Electronic Industries Association Standard RS232C and CCITT Recommendations V.24. The leads supported are:

Protective Ground	Signal Ground
Transmitted Data	Data Terminal Ready
Received Data	Request to Send

Any cable compatible with the DEC DL-11B is compatible with the QUADRASYNC.

POWER REQUIREMENTS

1.950 amps @ + 5V
0.100 amps @ + 15V
0.200 amps @ - 15V

DATA RATES

The QUADRAASYNC offers seven independently selectable baud rates for each channel. The transmitter and receiver of each channel operate at the identical baud rate. The baud rates are:

NOTES:

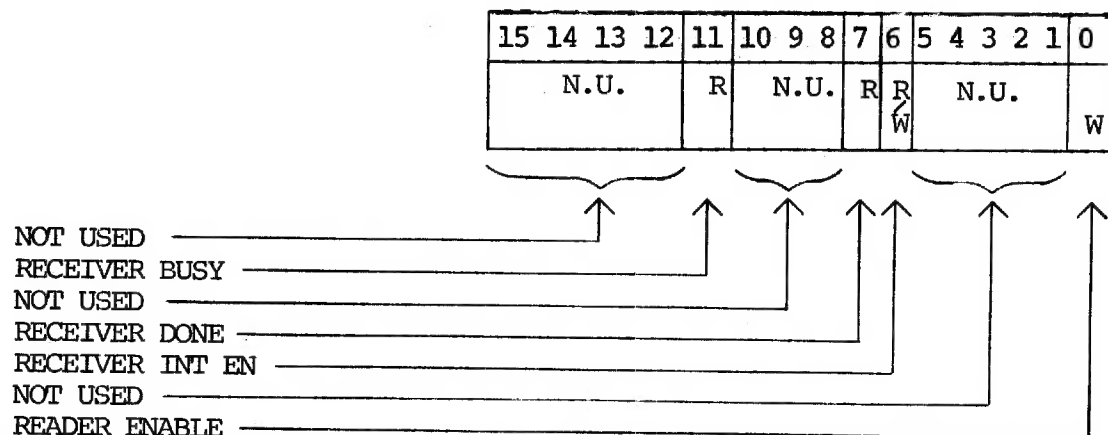
BAUD RATE	SWITCH POSITION
9600 baud	7
4800 baud	6
2400 baud	5
1200 baud	4
600 baud	3
300 baud	2
150 baud	1
19.2 k B	8
NC	9
NC	10

- 1) Switch position 1 is when the arrow ON switch is pointed directly toward UART.
- 2) Ascending positions are in clockwise direction.
- 3) CH 1 switch is closest to center of board and ascending to CH 4 on left side of board.

PROGRAMMING SPECIFICATIONS

RECEIVER STATUS REGISTERS: 77XXX0

Receiver Status Register #1 X00
 Receiver Status Register #2 X01
 Receiver Status Register #3 X10
 Receiver Status Register #4 X11



BIT

DESCRIPTION AND OPERATION

15-12

NOT USED. READ AS ZERO.

11

READ ONLY. SET WHEN UART RECEIVES VALID START BIT. CLEARED BY BIT 7 WHEN SET, AND BY INIT.

10-8

NOT USED. READ AS ZERO.

7

READ ONLY. SET WHEN UART HAS INCOMING DATA ASSEMBLED AND READY FOR TRANSFER. CLEARED BY SETTING BIT 0 (READER ENABLE), ADDRESSING READER BUFFER, OR BY INIT.

6

READ/WRITE. WHEN SET CAUSES AN INTERRUPT REQUEST EACH TIME BIT 7 (RECEIVER DONE IS SET). CLEARED BY PROGRAM OR INIT.

5-1

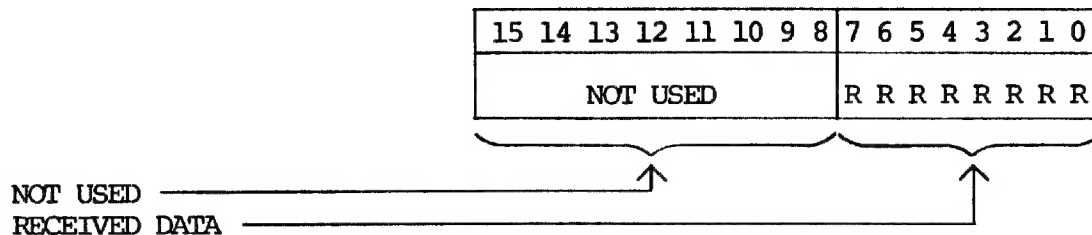
NOT USED. READ AS ZERO.

0

WRITE ONLY. READ AS ZERO. WHEN SET, CLEARS BIT 7 (RECEIVER DONE).

RECEIVER DATA BUFFER REGISTERS: 77XXX2

Receiver Data Buffer #1 X00
 Receiver Data Buffer #2 X01
 Receiver Data Buffer #3 X10
 Receiver Data Buffer #4 X11



BIT

DESCRIPTION AND OPERATION

15-8

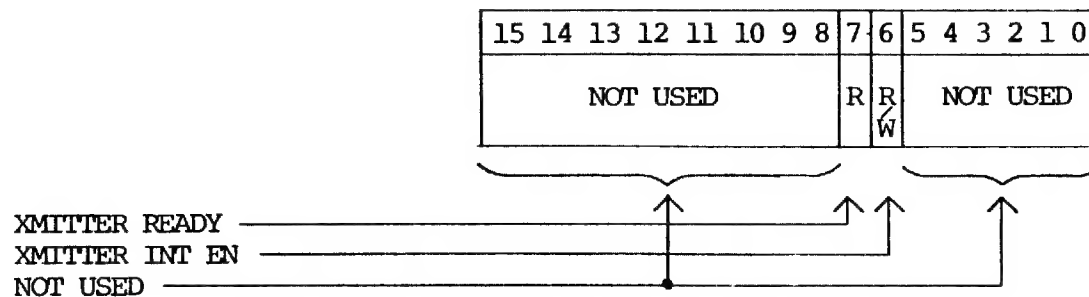
NOT USED. READ AS ZERO.

7-0

RECEIVED DATA. READ ONLY. LAST COMPLETE CHARACTER ASSEMBLED BY THE UART. CHARACTERS ARE RIGHT JUSTIFIED WHEN CHARACTERS ARE LESS THAN 8 BITS.

TRANSMITTER STATUS REGISTERS: 77XXX4

Transmitter Status #1 X00
 Transmitter Status #2 X01
 Transmitter Status #3 X10
 Transmitter Status #4 X11



BIT

DESCRIPTION AND OPERATION

15-8

NOT USED. READ AS ZERO.

7

READ ONLY. SET WHEN TRANSMITTER CAN ACCEPT ANOTHER CHARACTER AND BY INIT. CLEARED WHEN A CHARACTER IS LOADED INTO THE TRANSMITTER BUFFER.

6

READ/WRITE. WHEN SET, WILL CAUSE AN INTERRUPT REQUEST WHENEVER BIT 7 IN THE TRANSMITTER STATUS REGISTER IS SET. CLEARED BY THE PROGRAM AND BY INIT.

5-0

NOT USED. READ AS ZERO.

TRANSMITTER BUFFER REGISTERS: 77XXX6

Transmitter Buffer #1 X00
 Transmitter Buffer #2 X01
 Transmitter Buffer #3 X10
 Transmitter Buffer #4 X11

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								W	W	W	W	W	W	W	W

NOT USED

TRANSMITTER DATA

BIT

DESCRIPTION AND OPERATION

7-0

WRITE ONLY. CONTAINS THE CHARACTER TO BE TRANSMITTED BY THE UART. WHEN FEWER THAN 8 DATA BITS, THE CHARACTER MUST BE RIGHT JUSTIFIED WHEN LOADED INTO THE TRANSMITTER BUFFER. A BIT SET WILL CAUSE A MARK TO APPEAR ON THE TRANSMITTED DATA LEAD FOR ONE BIT TIME. CLEARED BY INIT.

ADDRESS SELECTION															ADDRESS SWITCH SELECTION			REGISTER
S S S S S S S S S S S S S S S S															W W W W W W W W W W W W W W W W			
4 2 5 1 6 3																		
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	REGISTER
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	0	0	0	R C S R #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	0	1	0	R B U F #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	1	0	0	X C S R #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	1	1	0	X B U F #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	0	0	0	R C S R #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	0	1	0	R B U F #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	1	0	0	X C S R #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	1	1	0	X B U F #2
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	0	0	0	R C S R #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	0	1	0	R B U F #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	1	0	0	X C S R #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	1	1	0	X B U F #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	0	0	0	R C S R #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	0	1	0	R B U F #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	1	0	0	X C S R #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	1	1	0	X B U F #4

SW - OPEN = 0
 SW - CLOSED = 1

ADDRESS RANGE: 7 7 7 7 7 6 } 7 7 6 1 7 6 }
 7 7 6 6 7 6 } DL11-A,-B 7 7 5 6 1 0 } DL11-C,-D,-E
 7 7 6 5 0 0 } 7 7 4 0 0 0 }

ADDRESS IS NORMALLY SET FOR 776500

VECTOR ADDRESS:

S	S	S	S							
W	W	W	W							
7	10	9	8	SWITCH SELECTION						
8	7	6	5	4	3	2	1	0	VECTOR	
X	X	X	X	0	0	0	0	0	RCVR #1	
X	X	X	X	0	0	1	0	0	XMIT #1	
X	X	X	X	0	1	0	0	0	RCVR #2	
X	X	X	X	0	1	1	0	0	XMIT #2	
X	X	X	X	1	0	0	0	0	RCVR #3	
X	X	X	X	1	0	1	0	0	XMIT #3	
X	X	X	X	1	1	0	0	0	RCVR #4	
X	X	X	X	1	1	1	0	0	XMIT #4	

SW - OPEN = 1
SW - CLOSED = 0

VECTOR ADDRESSES ARE NORMALLY SET TO
774 THRU 740

VECTOR RANGE:

7 7 7 thru 0 0 0

CONNECTOR LIST

J1

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #1 SIGNAL GND	1
VV	CH #1 SIGNAL GND	2
TT	CH #1 +5 Vdc	3
DD	CH #1 EIA TERM. RDY	15
V	CH #1 EIA REQ TO SEND	23
J	CH #1 EIA REC DATA	33
F	CH #1 EIA XMIT DATA	35

J2

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #2 SIGNAL GND	1
VV	CH #2 SIGNAL GND	2
TT	CH #2 +5 Vdc	3
DD	CH #2 EIA TERM. RDY	15
V	CH #2 EIA REQ TO SEND	23
J	CH #2 EIA REC DATA	33
F	CH #2 EIA XMIT DATA	35

J3

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #3 SIGNAL GND	1
VV	CH #3 SIGNAL GND	2
TT	CH #3 +5 Vdc	3
DD	CH #3 EIA TERM. RDY	15
V	CH #3 EIA REQ TO SEND	23
J	CH #3 EIA REC DATA	33
F	CH #3 EIA XMIT DATA	35

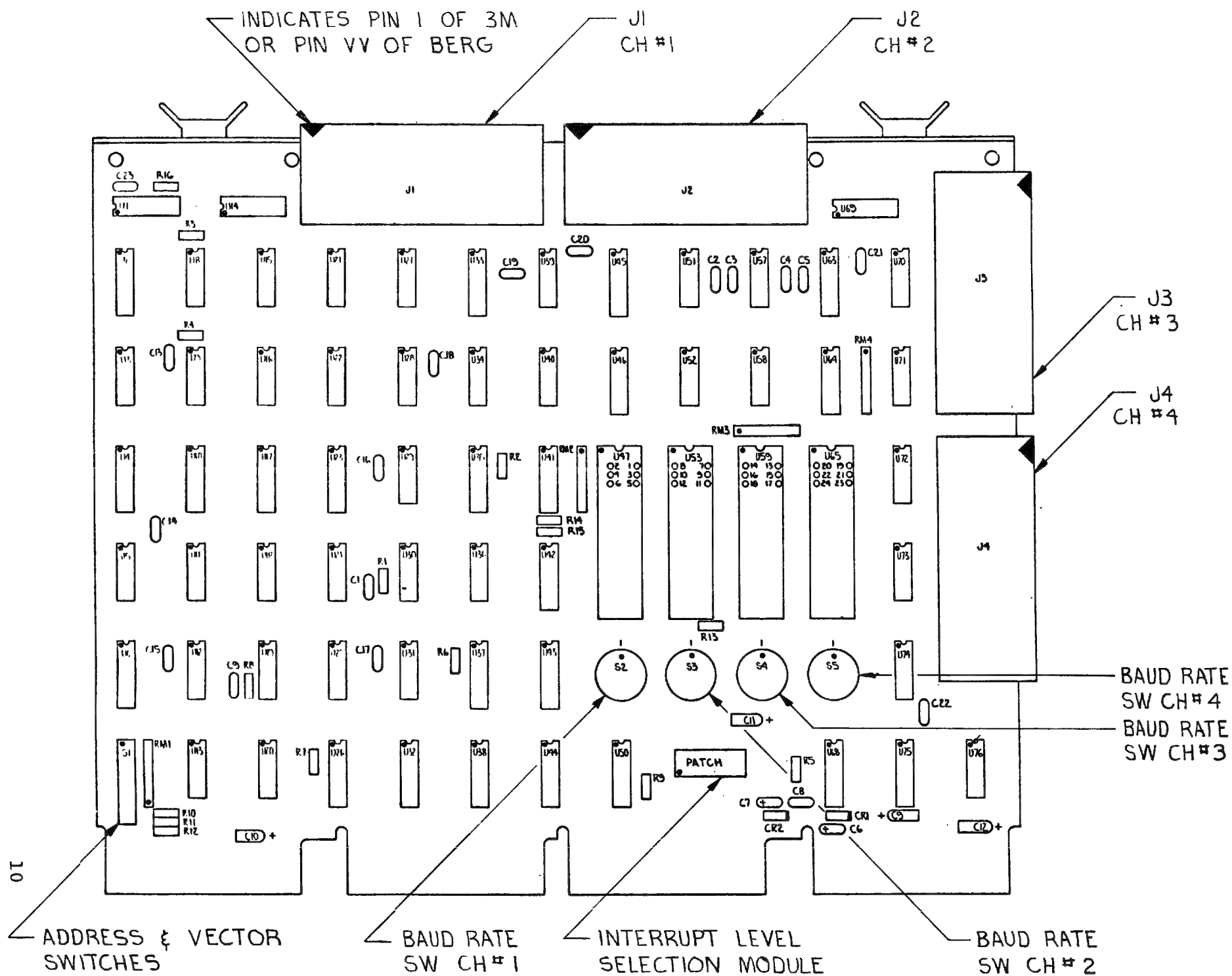
J4

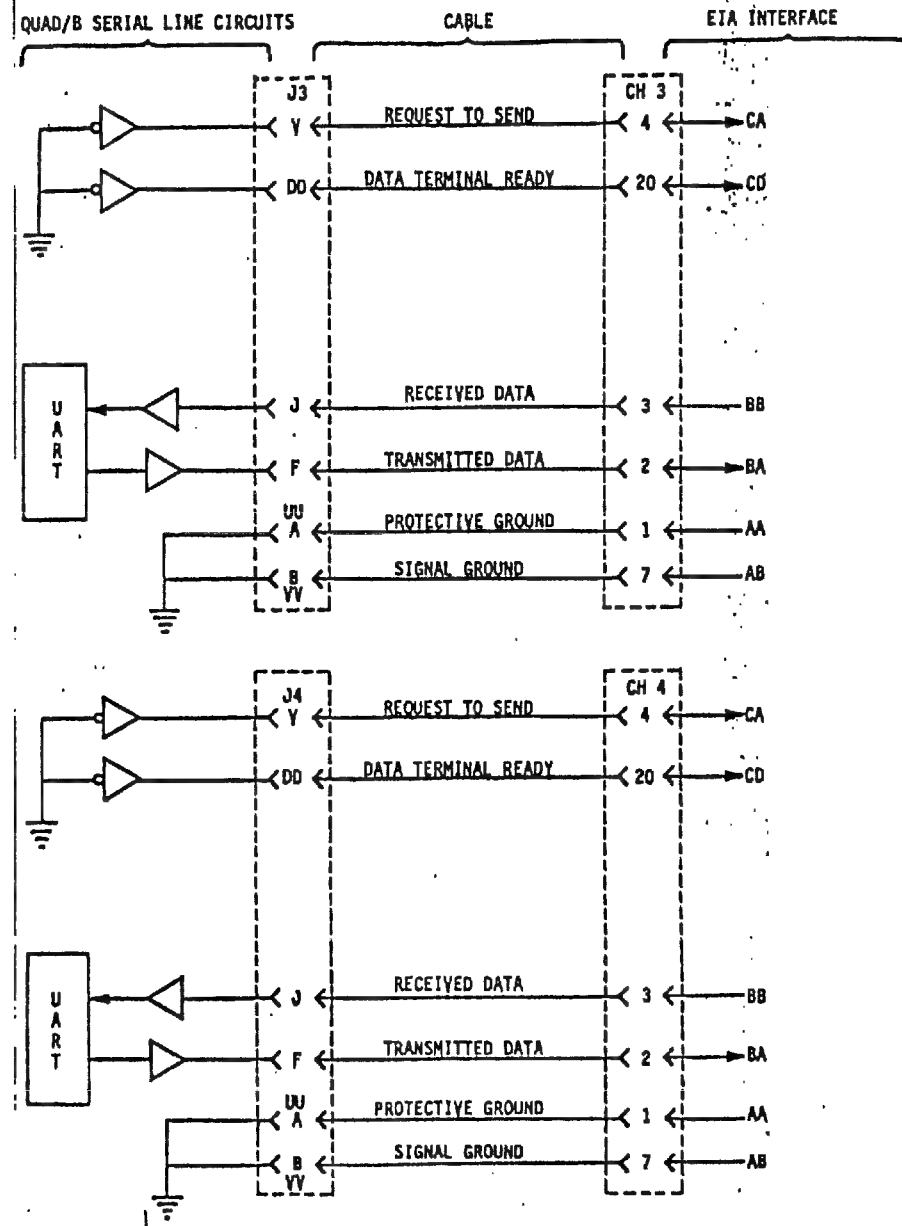
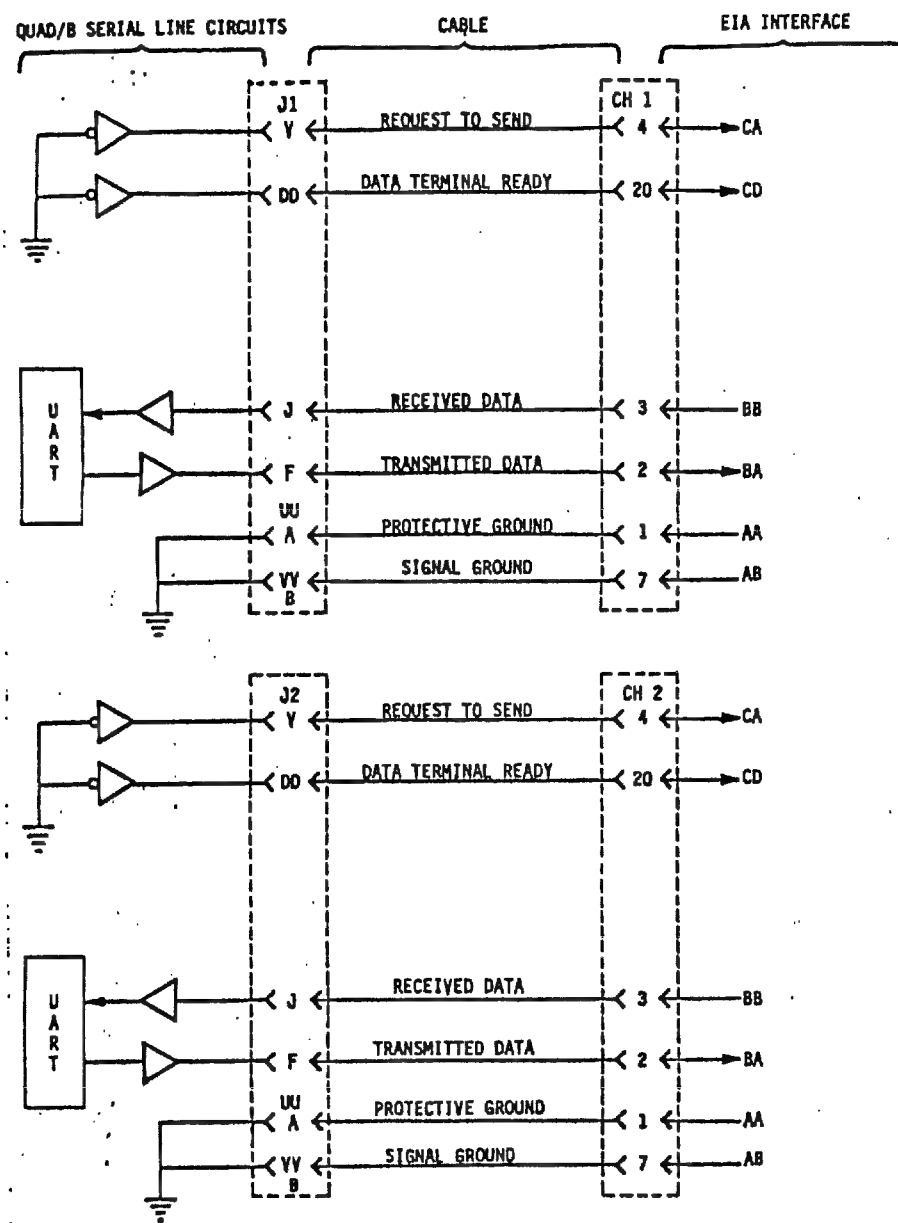
BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #4 SIGNAL GND	1
VV	CH #4 SIGNAL GND	2
TT	CH #4 +5 Vdc	3
DD	CH #4 EIA TERM. RDY	15
V	CH #4 EIA REQ TO SEND	23
J	CH #4 EIA REC DATA	33
F	CH #4 EIA XMIT DATA	35

INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	JUMPER FROM					
	PIN 1	PIN 3	PIN 5	PIN 7	PIN 13	PIN 15
LEVEL 4	16	4	6	8	9	2
LEVEL 5	2	16	6	8	10	4
LEVEL 6	2	4	16	8	11	6
LEVEL 7	2	4	6	16	12	8

- NOTE:
- 1) CONNECTION TO BE MADE BY JUMPER WIRES ADDED OR REMOVED ACCORDING TO THE ABOVE CHART.
 - 2) NORMALLY SET FOR LEVEL 4.





EIA INTERFACE

REV	ECO	DESCRIPTION	ORIG.	DATE	APPD.
A		REL		10-28-76	
B		SEE E.O.		12-10-76	
C		SEE E.O.		2-11-77	

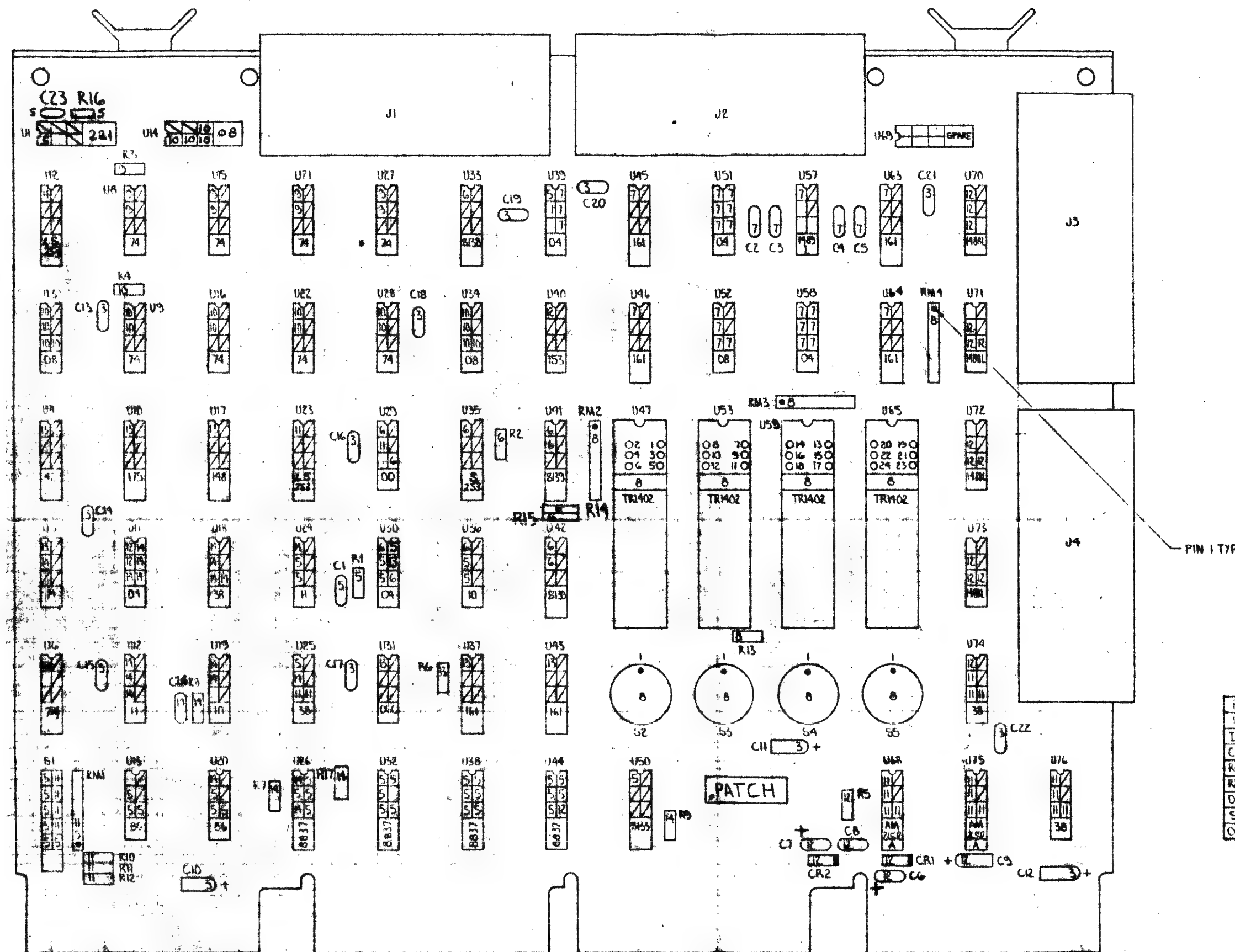
2 ALL CAPACITORS ARE IN MICRO-FARADS.
1. ALL RESISTORS ARE 1/4W. 5 %.
NOTE: UNLESS OTHERWISE SPECIFIED.

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QUADRA SYNC
10015003 C
SHT. 1 OF 15

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	REL	12-21-76	
B	SEE E.O.	12-10-76	
C	SEE E.O.	2-11-77	



REFERENCE DESIGNATION CHART		
TYPE	LAST USED	NOT USED
I.C.	U76	
CAPACITOR	C24	
RESISTOR	R17	
RES. MOD.	RM4	
DIODE	CR2	
SWITCH	S5	
OSCILLATOR	U31	

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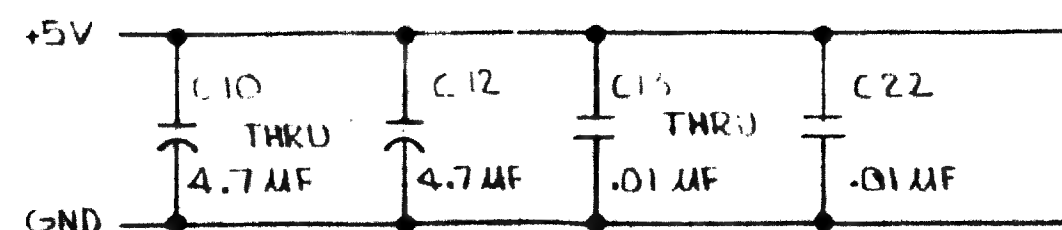
APPROVALS		DATE	
DESIGNED		DATE	
CHECKED		DATE	
APPROVED		DATE	
SCHEMATIC		QUADRASYNC	
-		D 10015003	
DO NOT SCALE DRAWING		SHEET 2 OF 15	

SHT	2	F	1	SHT
	+5V	A		
		B		
	GND	C		
		D	BUS BBSY-L	14
		E		
		F		
		H		
		J		
		K		
		L		
		M	BUS-INTR-L	14
		N		
		P		
		R		
		S		
14	BUS SACK-L	T		
		U		
		V		

SHT	2	E	1	SHT
	+5V	A		
		B		
5	GND	C	A12-L	5
5	A15-L	D	A17-L	5
5	A16-L	E	MSYN-L	5
5	BUS CI-L	F	A02-L	5
5	A00-L	H	A01-L	5
5	BUS CO-L	J	BUS SSYN-L	5
5	A13-L	K	A14-L	5
		L	A11-L	5
		M		
5	A08-L	N		
5	A07-L	P	A10-L	5
		R	A09-L	5
		S		
		T		
5	A04-L	U	A06-L	5
5	A03-L	V	A05-L	5

SHT	2	D	1	SHT
	+5V	A		
		B		
	GND	C		
		D		
		E		
		F		
		H		
		J		
15	B67-IN	K		
15	B67-OUT	L	BUS INIT-L	12
15	B66-IN	M		
15	B66-OUT	N		
15	B65-IN	P		
15	B65-OUT	R		
15	B64-IN	S		
15	B64-OUT	T		
		U		
		V		

SHT	2	C	1	SHT
	+5V	A		
		B		
	GND	C		
		D		
		E		
		F		
		H		
		J		
		K		
11	D08-L	L		
11	D07-L	M		
11	D04-L	N		
11	D05-L	P		
11	D01-L	R		
11	D00-L	S		
11	D03-L	T		
11	D02-L	U		
11	D06-L	V		



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17150-2-0
SHT 2 OF 15

SHT		J1				SHT
	GND	1	UU	VV	2	GND
		3	SS	TT	4	+5V
		5	PP	RR	6	
		7	MM	NN	8	
		9	KK	LL	10	
		11	HH	JJ	12	
		13	EE	FF	14	
		15	CC	DD	16	RDY-1
		17	AA	BB	18	
		19	Y	Z	20	
		21	W	X	22	
		23	U	V	24	SEND-1
		25	S	T	26	
		27	P	R	28	
		29	M	N	30	
		31	K	L	32	
		33	H	J	34	REC DATA-1
		35	E	F	36	DATA-1
		37	C	D	38	
	GND	39	A	B	40	GND

DTK

RTS

RD

TD

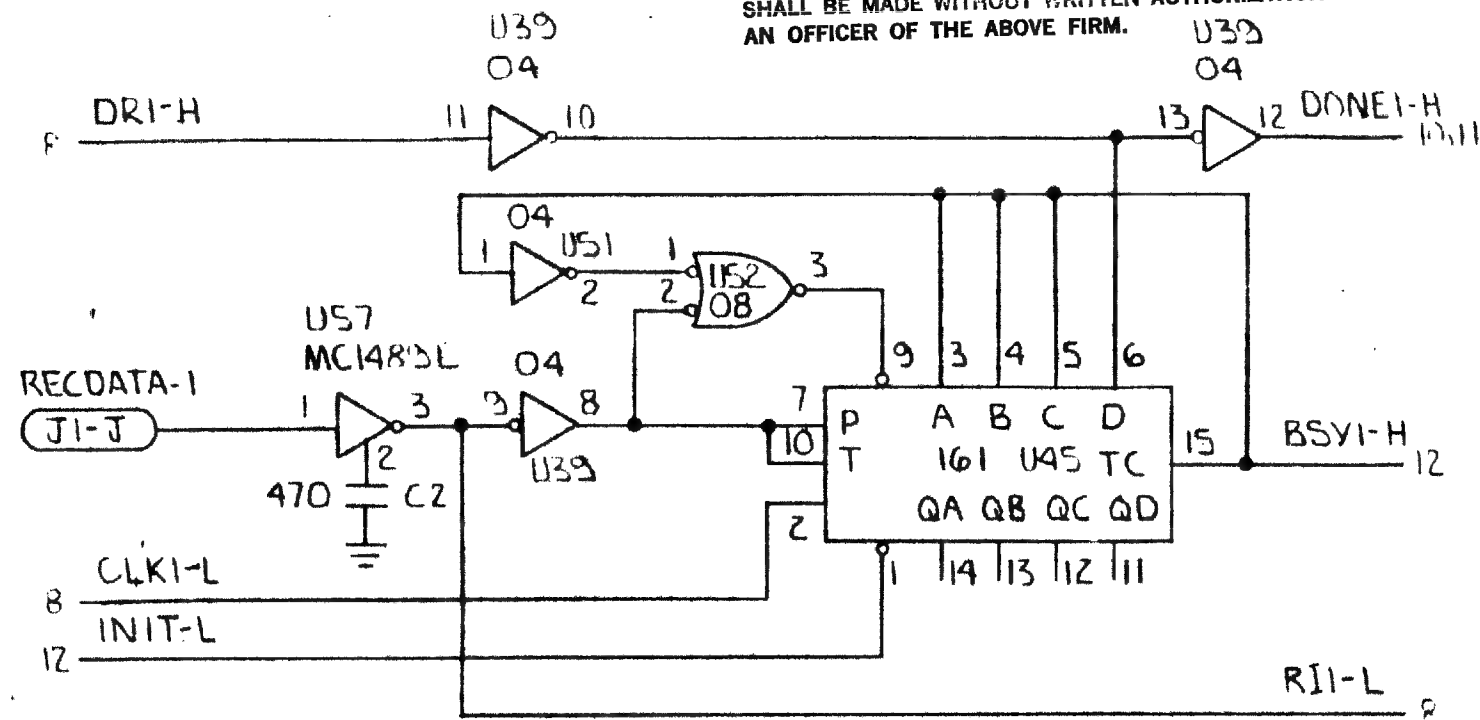
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	GND	1	UU	VV	2	GND
		3	SS	TT	4	+5V
		5	PP	RR	6	
		7	MM	NN	8	
		9	KK	LL	10	
		11	HH	JJ	12	
		13	EE	FF	14	
		15	CC	DD	16	RDY-3
		17	AA	BB	18	
		19	Y	Z	20	
		21	W	X	22	
		23	U	V	24	SEND-3
		25	S	T	26	
		27	P	R	28	
		29	M	N	30	
		31	K	L	32	
		33	H	J	34	REC DATA-3
		35	E	F	36	DATA-3
		37	C	D	38	
	GND	39	A	B	40	GND

SHT		J2				SHT
	GND	1	UU	VV	2	GND
		3	SS	TT	4	+5V
		5	PP	RR	6	
		7	MM	NN	8	
		9	KK	LL	10	
		11	HH	JJ	12	
		13	EE	FF	14	
		15	CC	DD	16	RDY-2
		17	AA	BB	18	
		19	Y	Z	20	
		21	W	X	22	
		23	U	V	24	SEND-2
		25	S	T	26	
		27	P	R	28	
		29	M	N	30	
		31	K	L	32	
		33	H	J	34	REC DATA-2
		35	E	F	36	DATA-2
		37	C	D	38	
	GND	39	A	B	40	GND

SHT		J4				SHT
	GND	1	UU	VV	2	GND
		3	SS	TT	4	+5V
		5	PP	RR	6	
		7	MM	NN	8	
		9	KK	LL	10	
		11	HH	JJ	12	
		13	EE	FF	14	
		15	CC	DD	16	RDY-4
		17	AA	BB	18	
		19	Y	Z	20	
		21	W	X	22	
		23	U	V	24	SEND-4
		25	S	T	26	
		27	P	R	28	
		29	M	N	30	
		31	K	L	32	
		33	H	J	34	REC DATA-4
		35	E	F	36	DATA-4
		37	C	D	38	
	GND	39	A	B	40	GND

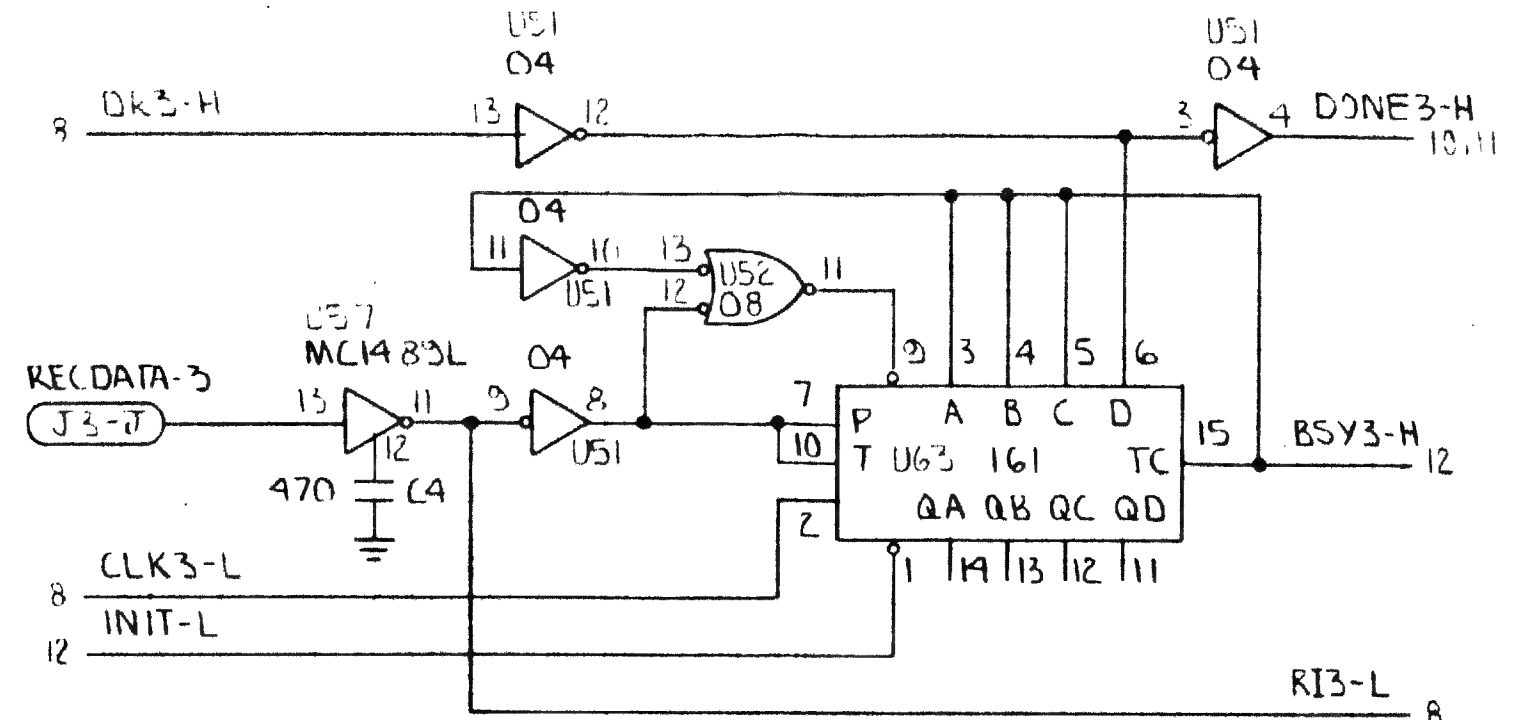
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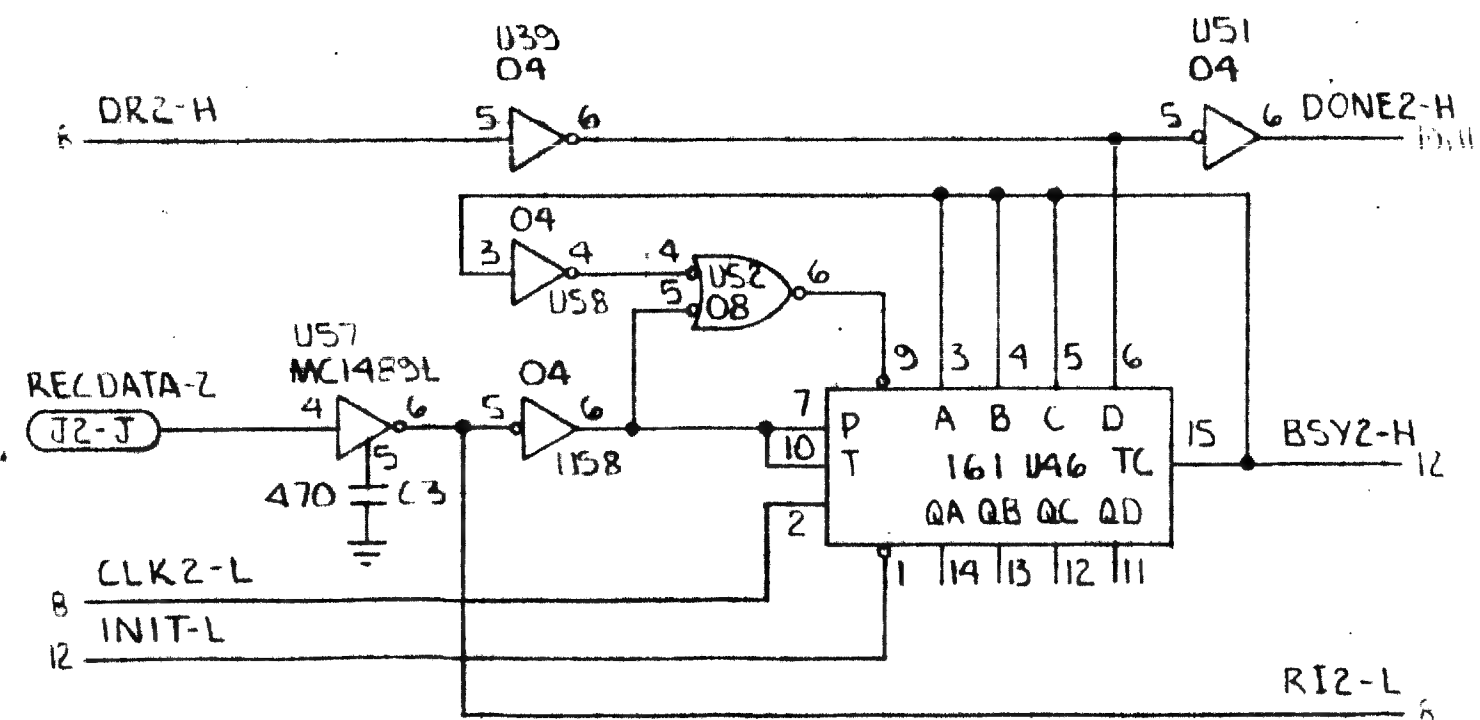
EIA RECEIVER 1 INPUT

BUSY DETECTION 1



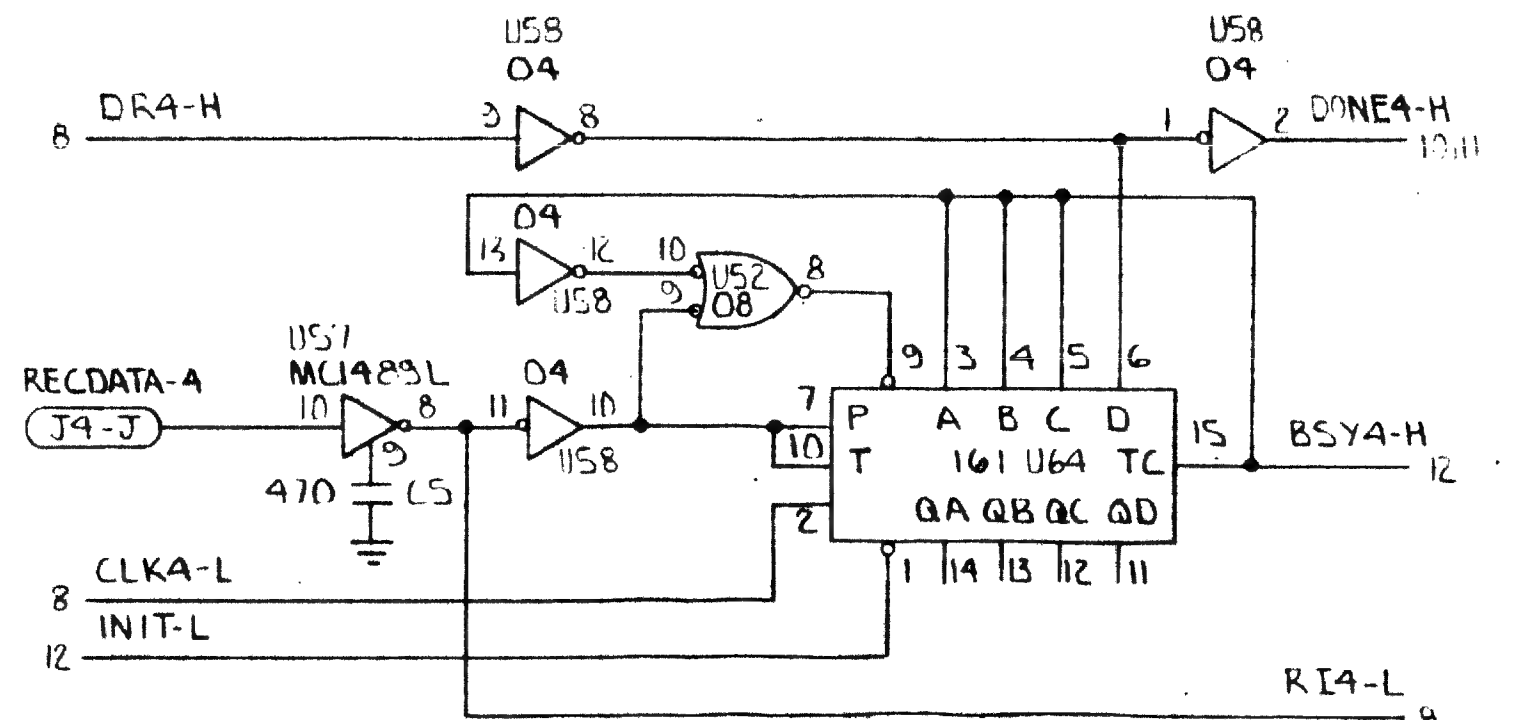
EIA RECEIVER 3 INPUT

BUSY DETECTION 3



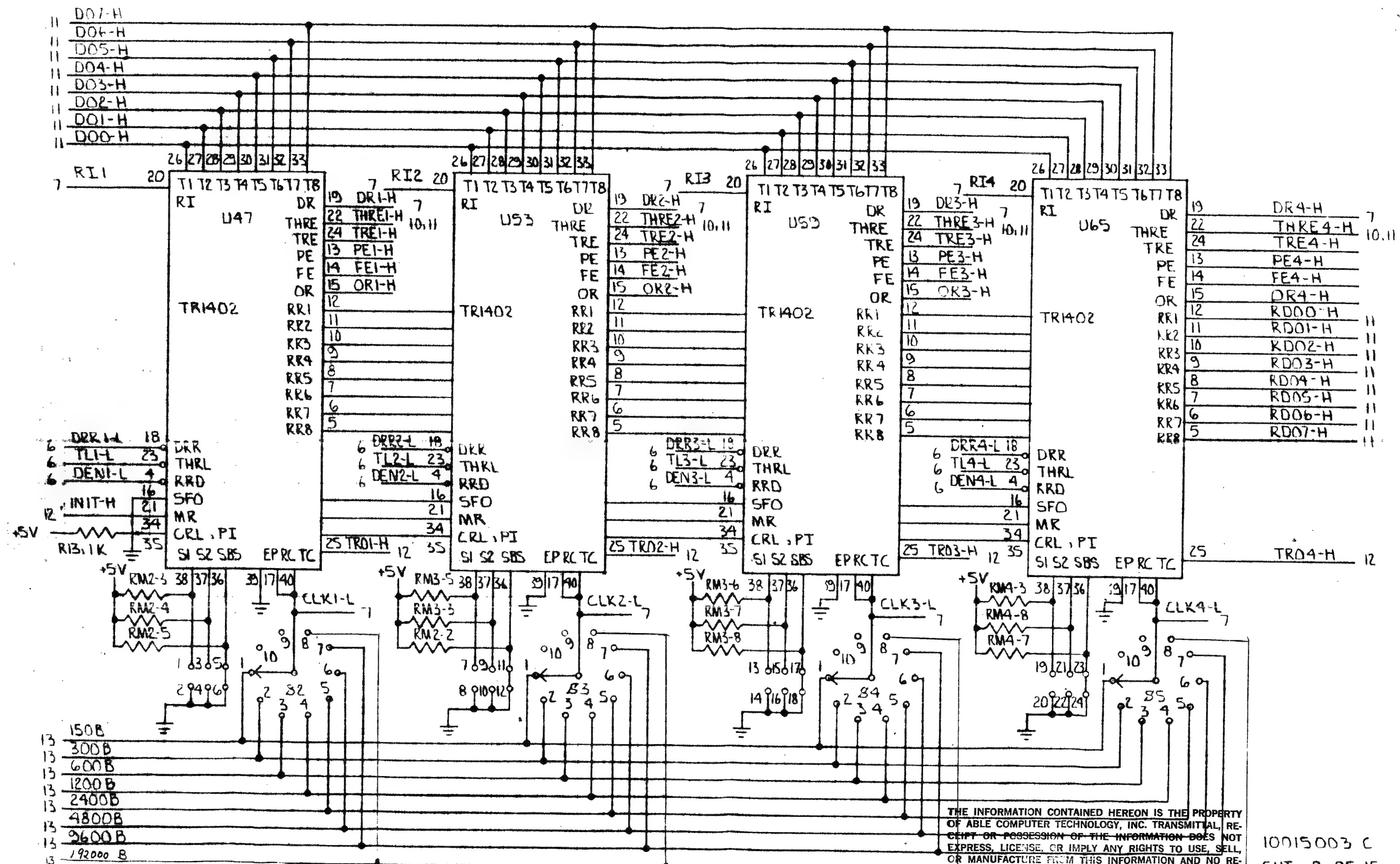
EIA RECEIVER 2 INPUT

BUSY DETECTION 2

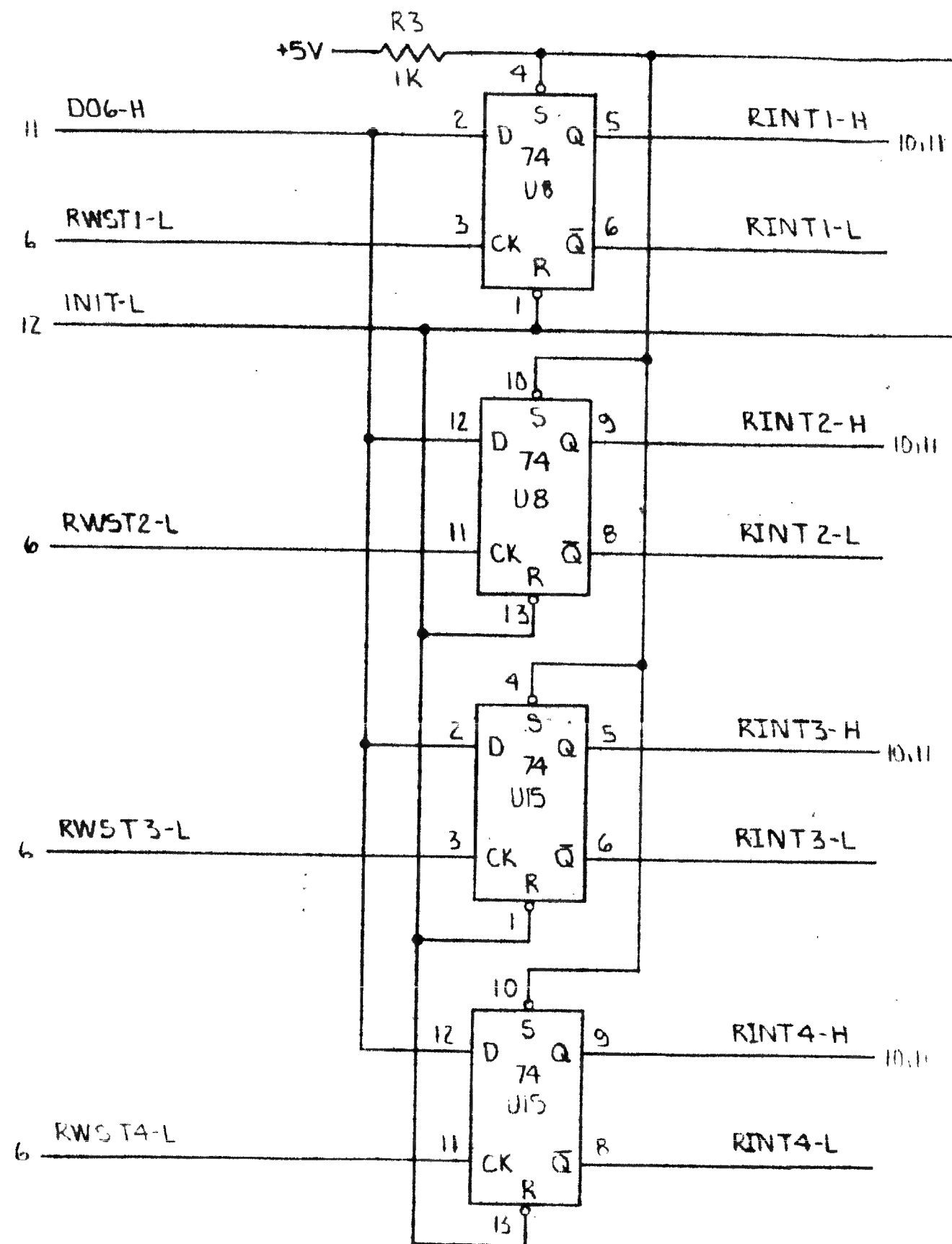


EIA RECEIVER 4 INPUT

BUSY DETECTION 4

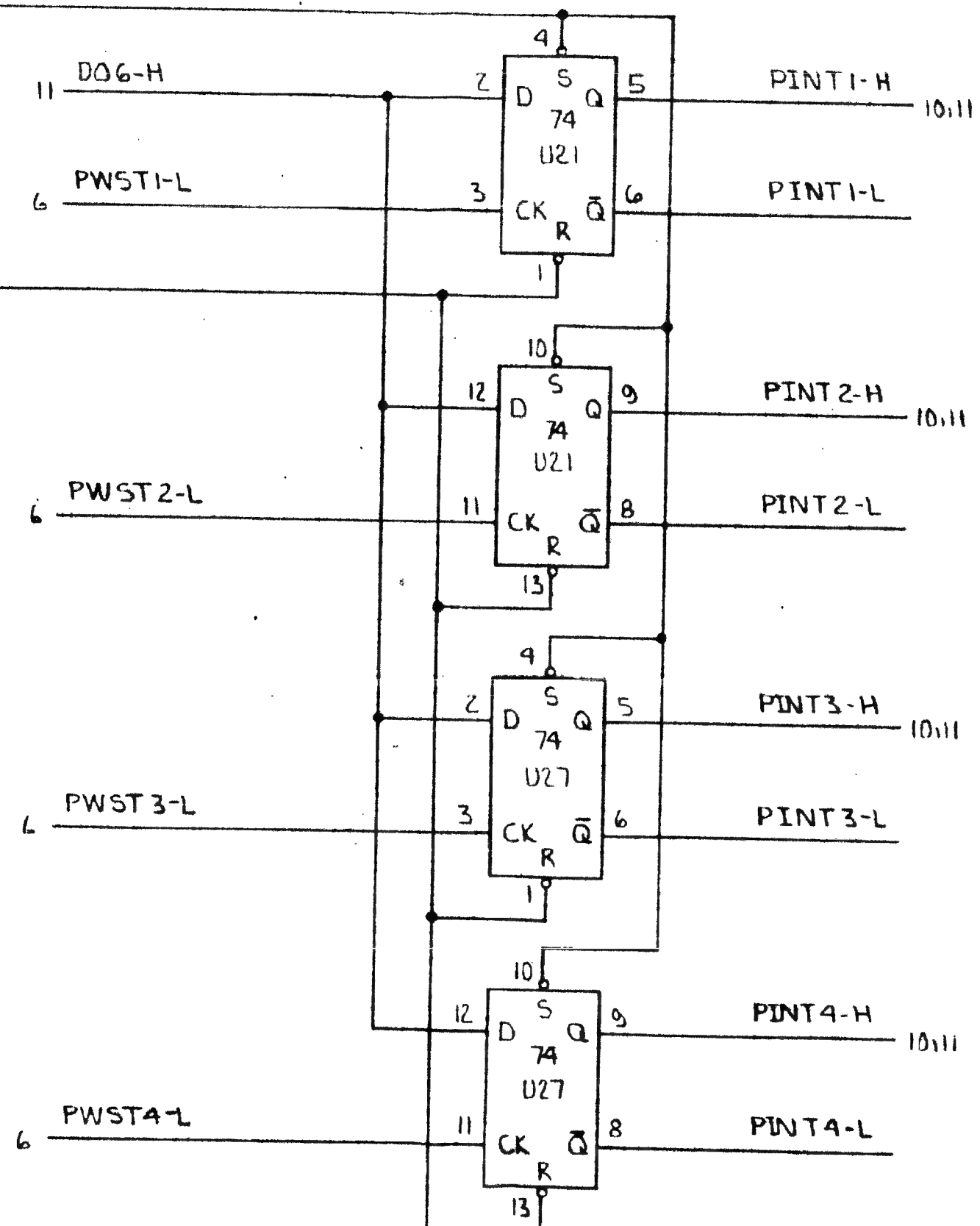


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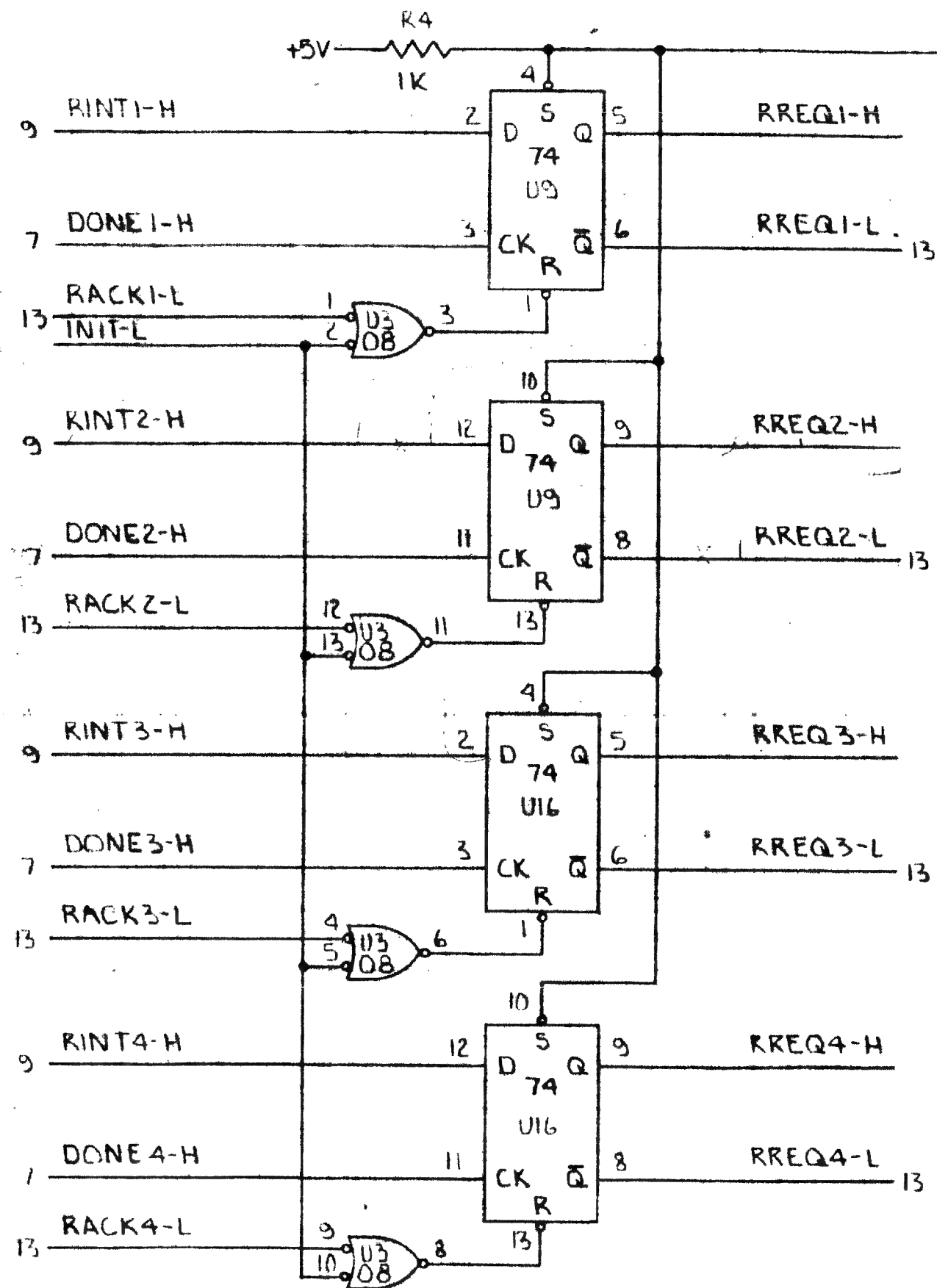
RECEIVER INTERRUPT ENABLE

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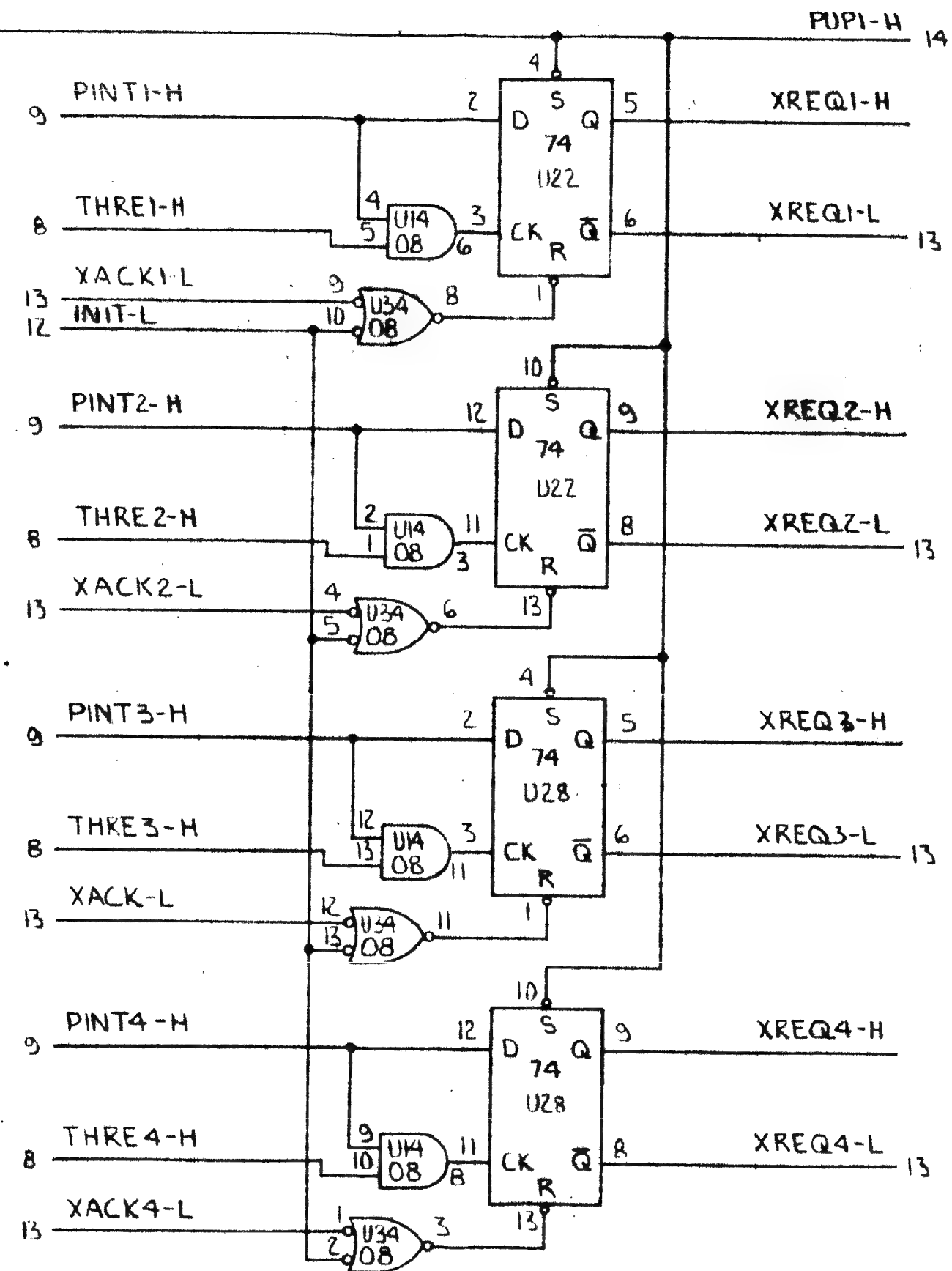
XMITTER INTERRUPT ENABLE

10015003 C
SHT. 9 OF 15



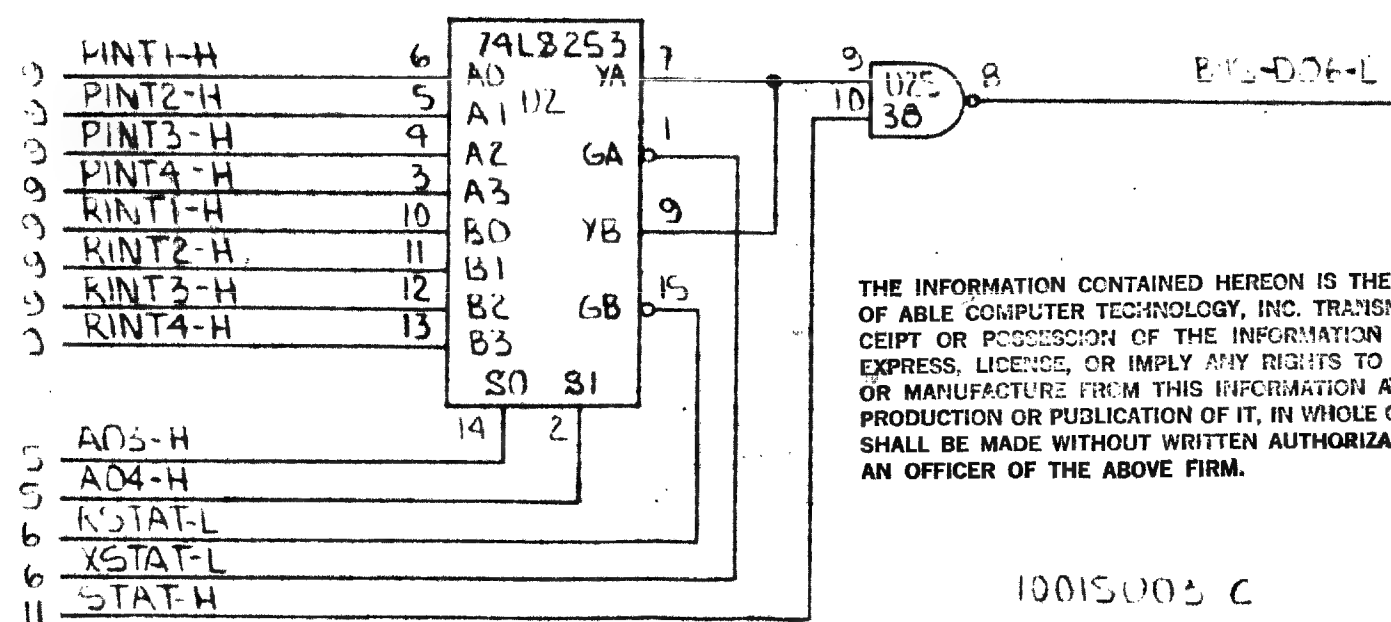
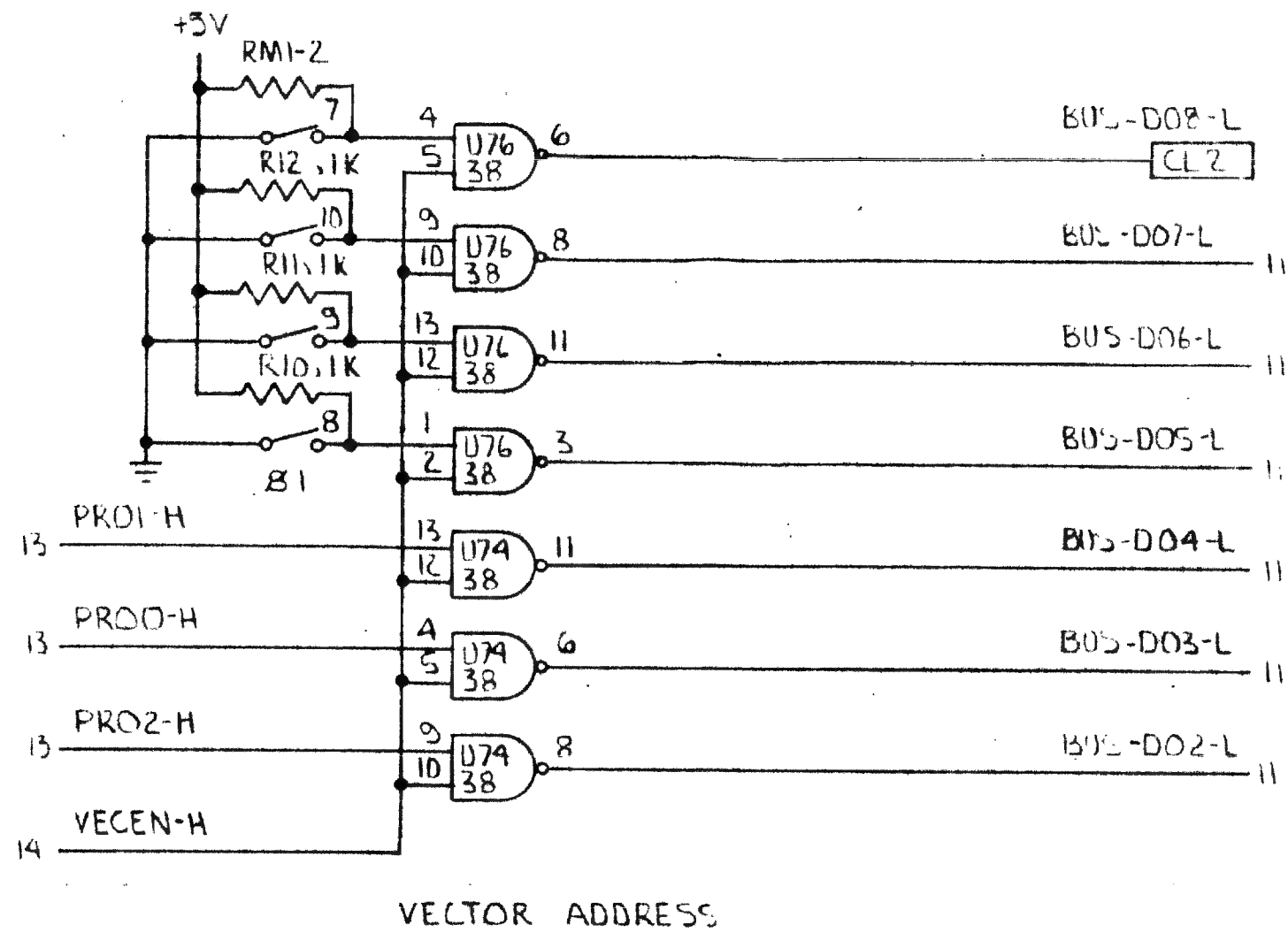
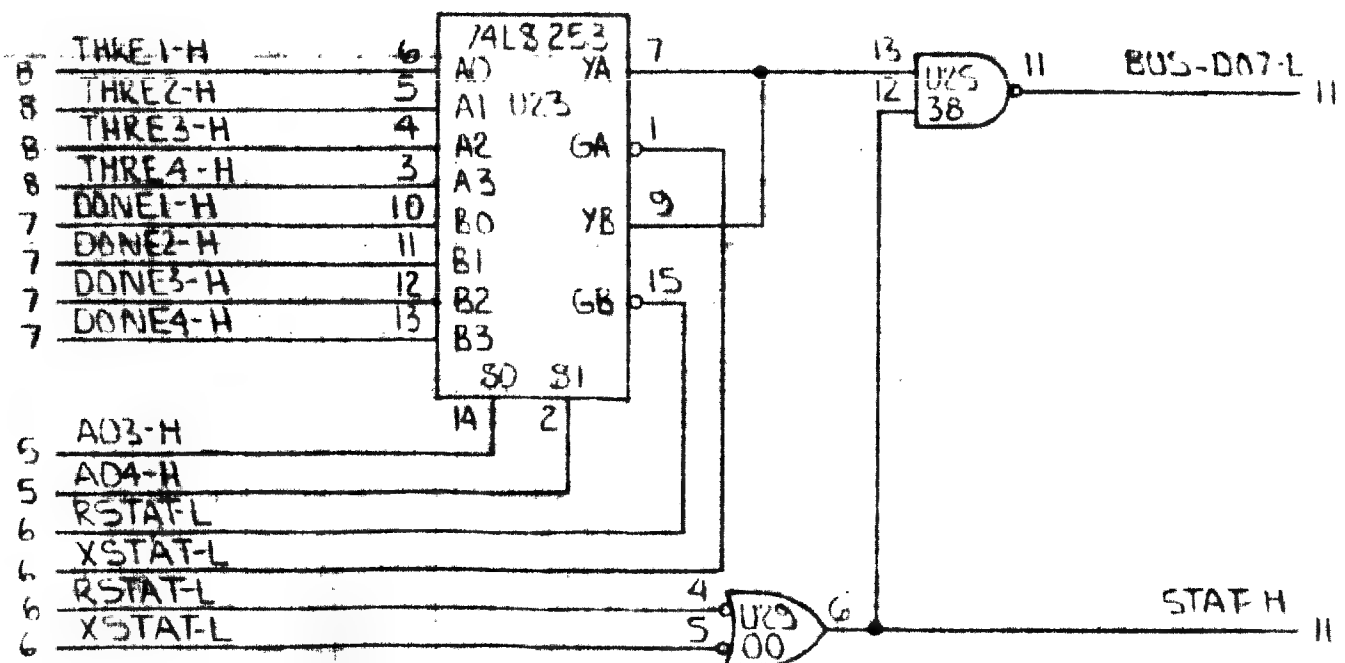
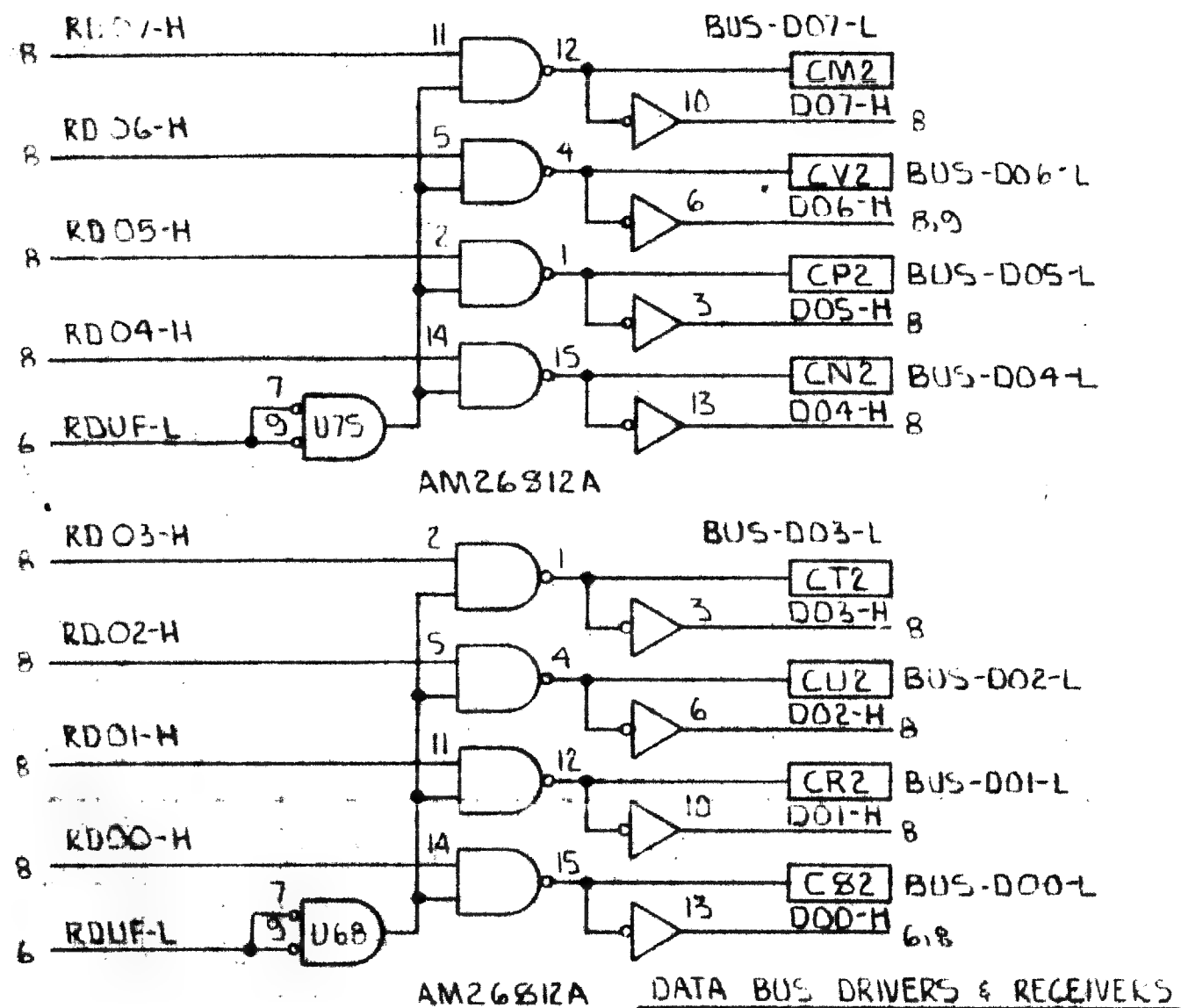
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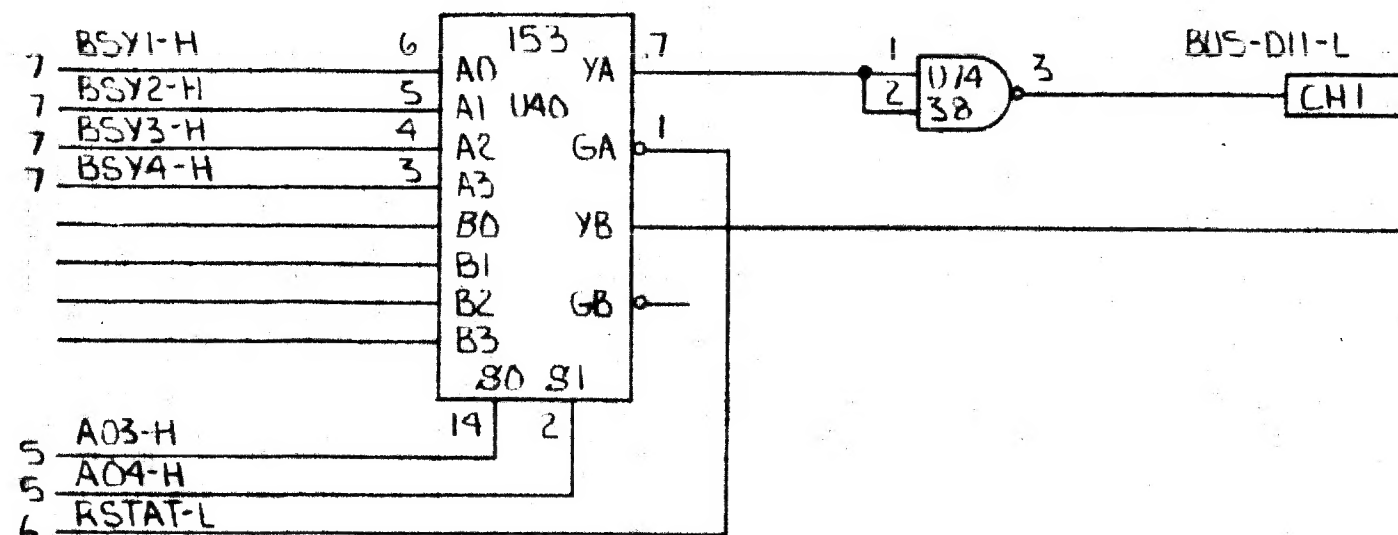
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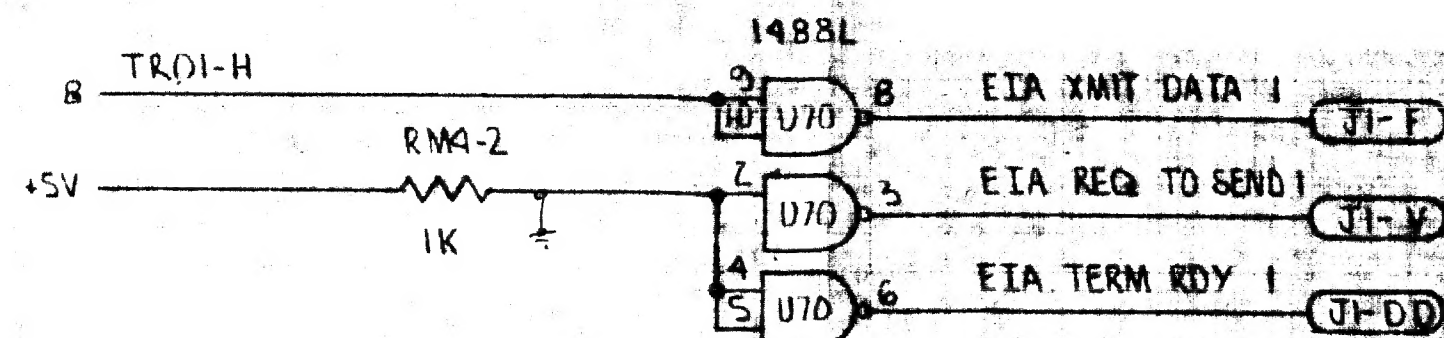
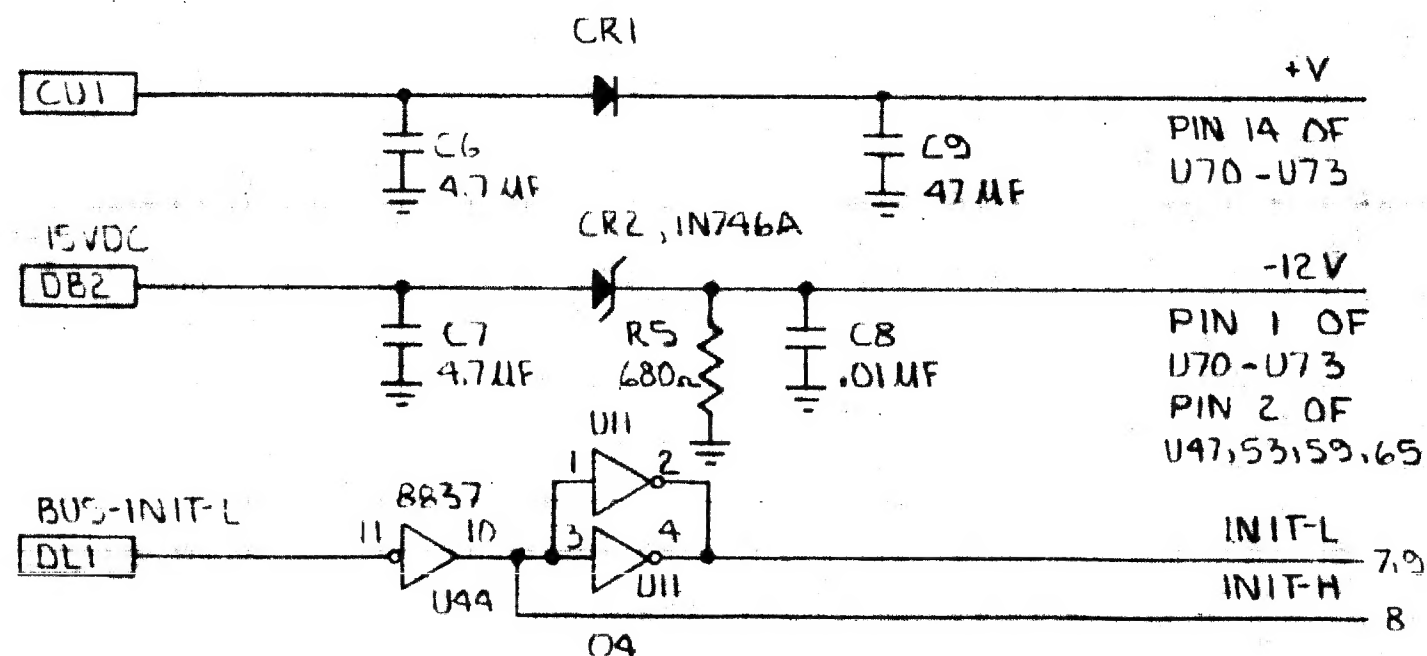


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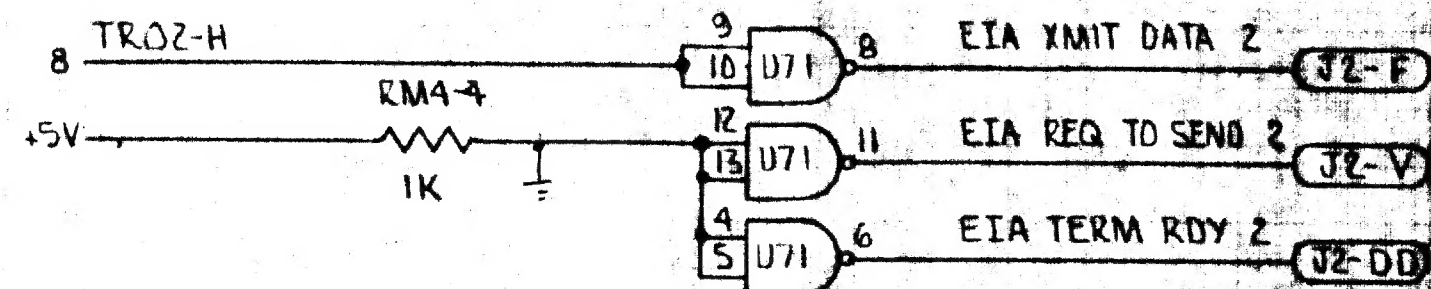
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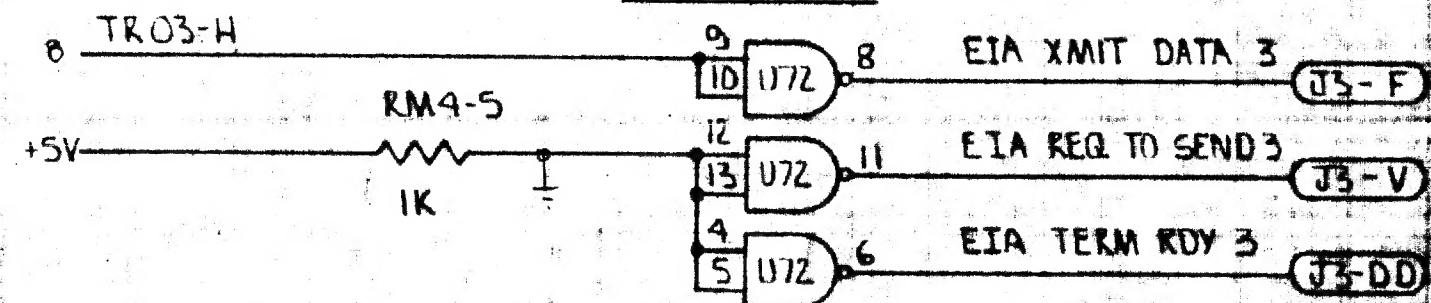
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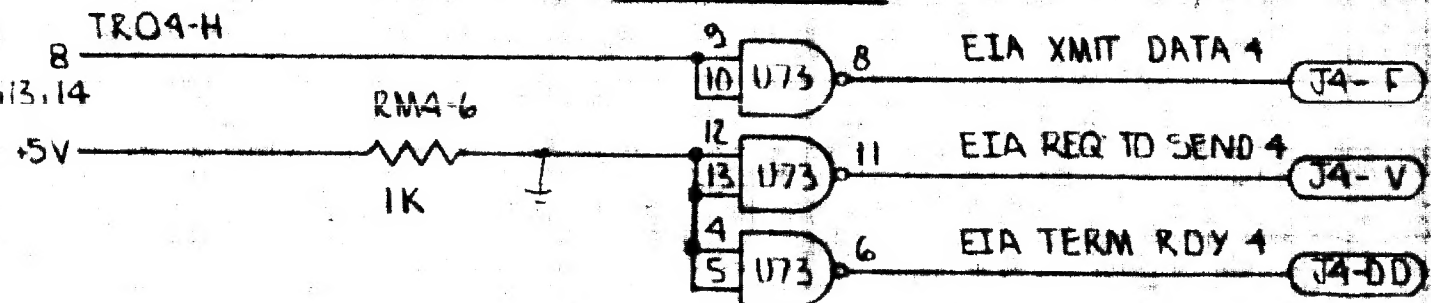
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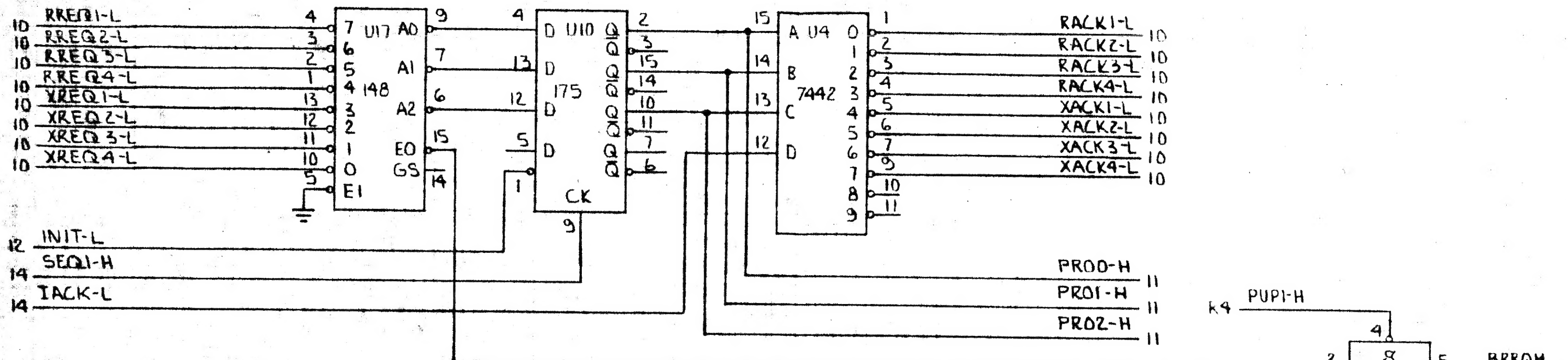
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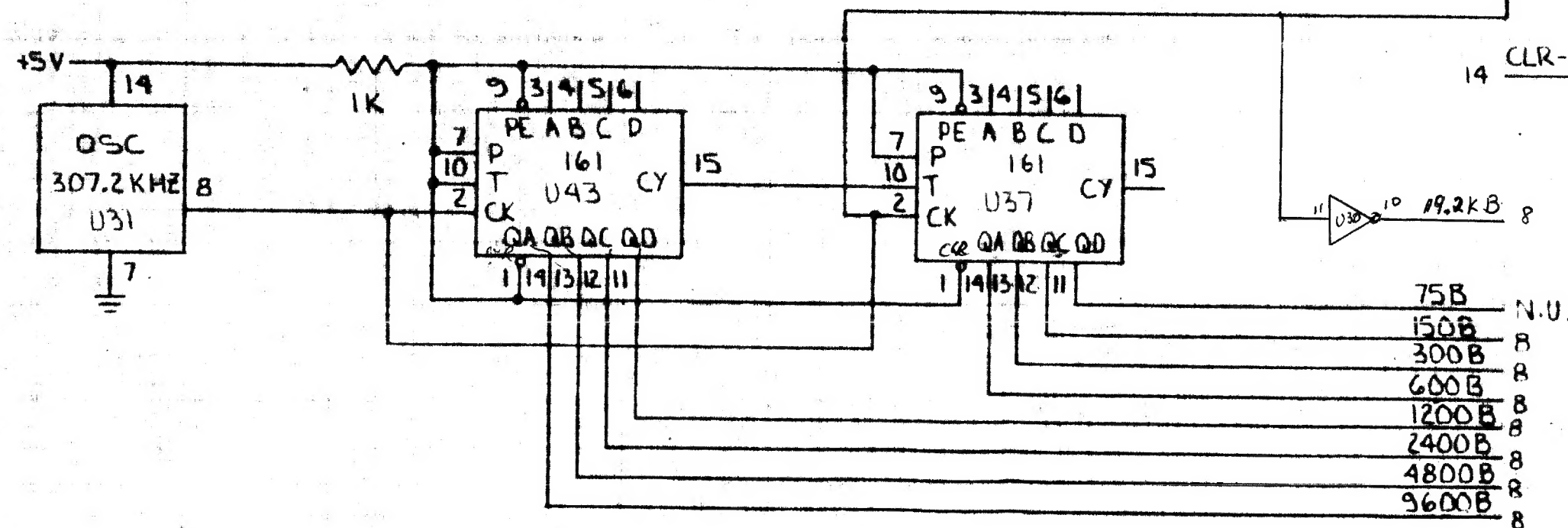
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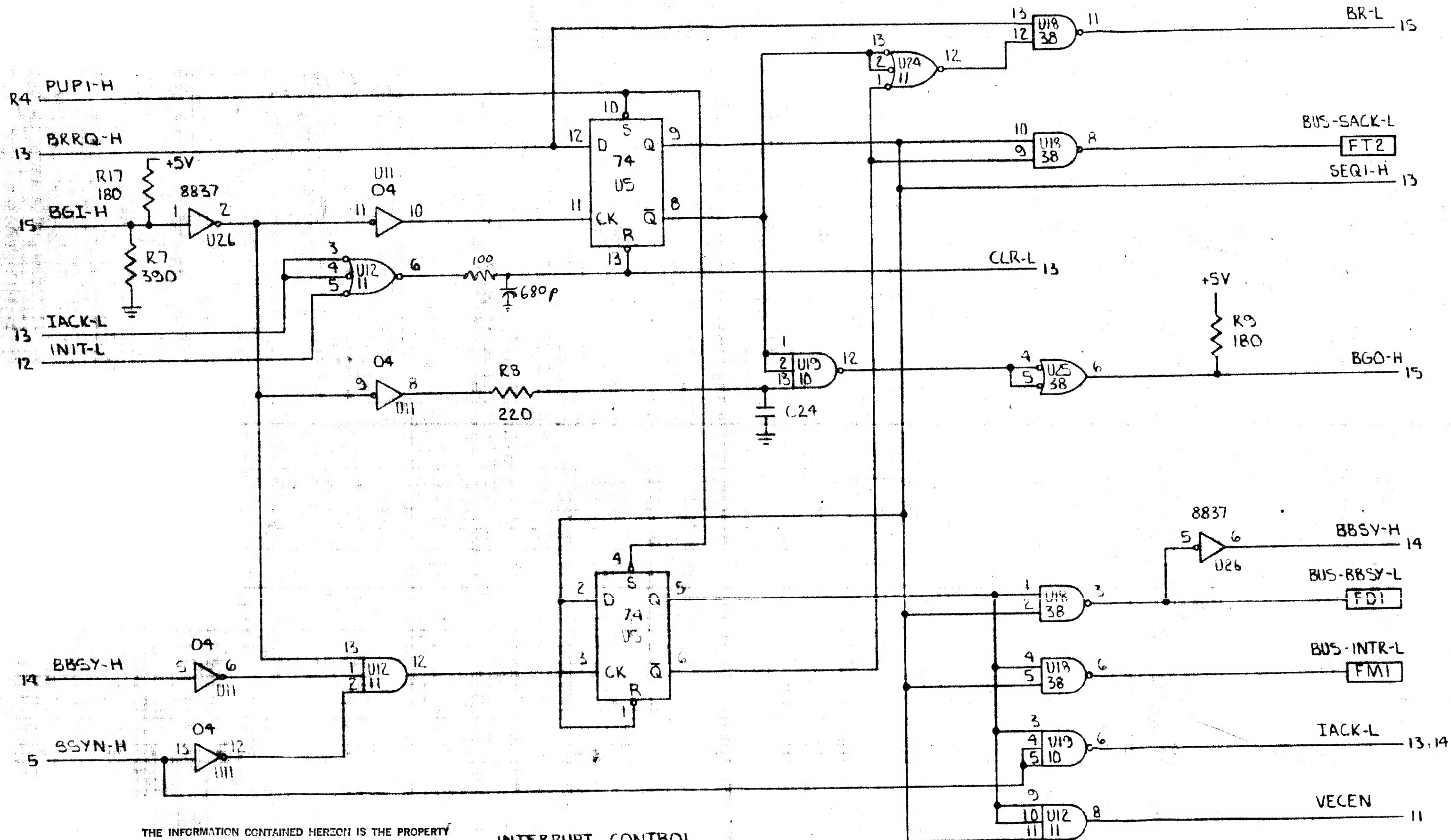


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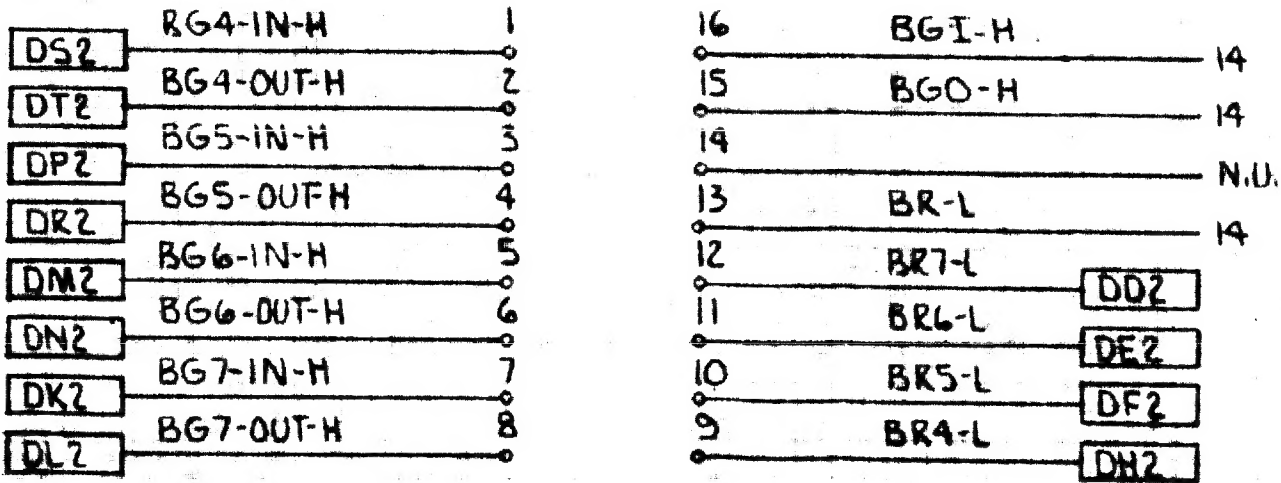


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